CDF Run IIb Silicon: Electrical Performance and Deadtime-less Operation

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***Abstract*— The main building block and readout unit of the planned CDF Run IIb silicon detector is a "stave", a highly integrated mechanical, thermal and electrical structure. One of its characteristic features is a copper-on-Kapton flexible cable for power/high voltage/data transmission and control signals that is placed directly below the silicon sensors. The dense packaging makes deadtime-less operation of the stave a challenge since coupling of bus cable activity into the silicon sensors must be suppressed efficiently. The stave design features relevant for deadtime-less operation are discussed. The electrical performance achieved with stave prototypes is presented.**

***Index Terms*— SVX4, CDF, Run IIb, Silicon tracker, deadtime-less.**

I. Introduction

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THE CDF collaboration has designed a new silicon tracking detector for the Tevatron's Run IIb. The new detector is designed to withstand the radiation levels of up to 20 MRad which are expected in Run IIb, while maintaining or improving the performance of the Run IIa silicon tracker [1], [2]. The main building block of the detector is a "stave", a highly integrated mechanical, thermal and electrical structure. Figure 1 shows a photograph of the stave inside a protective box. The stave is described in more detail elsewhere [3].

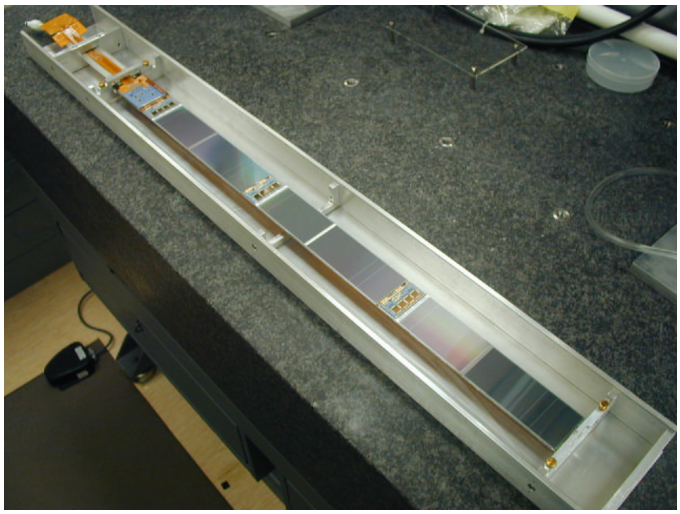

Fig. 1. Picture of the stave top side

CDF operates the silicon detector in a deadtime-less mode: data acquisition continues during digitization and readout. This increases the trigger bandwidth substantially. (The nominal CDF level 1 trigger rate is 50 kHz). While being highly desirable, deadtime-less operation may be challenging in terms of electrical performance. Critical effects are the possible coupling of the "noisy" digitization and readout activity into the analog (preamplifier and pipeline) section of the readout chip or the coupling of the control and data signals into the silicon sensor. The former effect has been minimized to a negligible level in the design of the SVX4 chip, the latter effect and its implication on detector performance is discussed here.

Particularly relevant for deadtime-less performance of the CDF Run IIb stave is the proximity of the bus cable to the silicon sensors. The silicon sensors are glued on top of the bus cable. This arrangement results in an exceptionally compact structure and offers major advantages for detector assembly. At the same time, pickup of bus cable activity into the silicon sensors is more likely, and the suppression of this effect requires particular care.

II. Electrical stave components

The main electrical stave components are: the SVX4 readout chips, the beryllia hybrids, the "Mini Portcard" (MPC), the silicon sensors, and the bus cables.

The **SVX4 chip** [4] is a radiation-hard mixed-signal ASIC fabricated in a 0.25 μm CMOS process. The chip consists of 128 charge-integrating preamplifiers, each with a 46-cell-deep analog pipeline and an analog-to-digital converter, and a digital readout unit for the 8-bit differential data bus and clock.

Sparsification of channels with signals exceeding a programmable sparsification threshold is a feature of the SVX4 and all CDF designs going back to the original SVX. The chip can perform real-time pedestal subtraction (RTPS) to suppress common-mode effects. The low resistivity substrate of the bulk CMOS process is exploited to carry all analog ground currents and effectively decouple the low noise analog section from the digital section of the chip.

The fine-pitch **beryllia hybrids** carry four SVX4 chips and 30 passive surface-mount components. They are glued on top of the silicon sensors, and are connected to the bus cable through a gap between adjacent sensors (see below) and via pitch adapters to the silicon strips. Digital and analog ground are connected to each other on the hybrid as required by the SVX4 chip design. This feature is not necessarily desirable from a system integration point of view, as will be discussed later. The hybrid also contains a simple RC high frequency filter of the sensor high voltage, and connects high voltage ground to hybrid ground.

The **beryllia Mini Portcard** [6] is located at the end of a stave. The MPC distributes high voltage, power, clock and control signals to the bus cable and thus the hybrids and sensors of the stave. The MPC contains five custom radiation-hard transceiver chips [5] which regenerate various signals, perform logic level conversions, and send the data stream to the data acquisition system. Important for deadtime-less operation and electrical stave performance are again the ground connections provided by the MPC. The digital grounds of the stave's six hybrids and the transceiver power supply ground are tied together at the MPC. Analog grounds are not connected on the MPC (but are connected to digital ground on each hybrid).

The **silicon sensors** are single-sided p^+-on-n AC-coupled microstrip detectors in a radiation-hard layout [7], fabricated by Hamamatsu Photonics. Pairs of sensors are daisy-chained together and read-out by the hybrid glued on top of one of the sensors.

The two stave **bus cables** are mounted on either side of the stave structure. They provide high voltage to the sensors; analog and digital power, as well as clock and control signals to the hybrids; and they transmit the data to the MPC. The cable is a 66 cm long Kapton/Copper/Aluminum flexible circuit laminate. The cable's 18 μm thick copper traces (1/2 oz. of copper per square foot) correspond to $\sim$ 8% of the stave's radiation length, which excludes the use of more than one trace layer. The aluminum layer, which contributes marginally to the material budget, serves as a shield between the copper trace layer and the silicon sensor high voltage backplane. It is separated in three sections corresponding to the three sensor plus hybrid groups. A detailed view of the bus cable layout in the region near the middle hybrid is shown in Figure 2. The wide traces correspond to power lines, the narrow ones to control, clock and data signals. Some of the power traces stop since they

have reached the hybrid they are meant to serve.

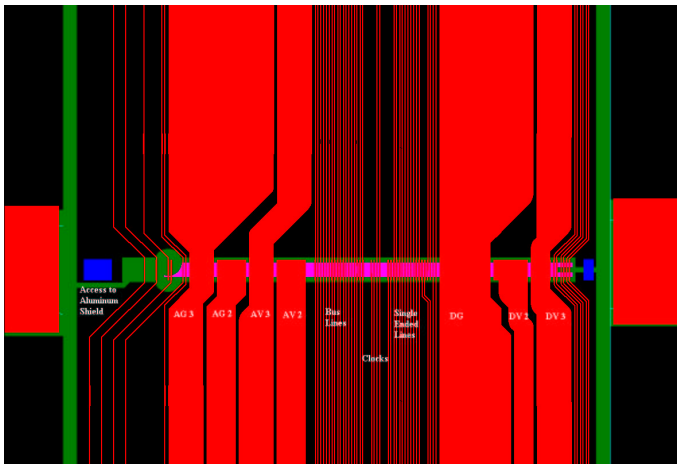

Fig. 2. Bus cable layout in one of the bond pad regions

Figure 3 shows the arrangement of these components on the stave and their electrical connection through wire bonds. The stave is essentially symmetric along its vertical axis with bus cables, sensors, and hybrids being placed on the bottom and the top side. There is only one MPC, however, which serves both sides of the stave. The bus cable traces and the sensor back plane are less than 125 μm apart.

The figure also illustrates that the bus cable traces (red) stop after reaching the third hybrid and (with the exception of the sensor high voltage) don't extend under the third pair of sensors. The three separate aluminum shield sections are also shown.

III. Importance of deadtime-less performance

The current performance of CDF staves operated in deadtime-less mode is illustrated in Figure 4. The figure shows the ADC counts recorded for an arbitrary channel as a function of time/mode of chip operation. The data is generated by repeatedly running a control pattern which collects pedestal data of the following operation modes of the chip: while the back-end section of the chip is idle; while it is digitizing; or while it is reading out. Each data point corresponds to a different charge integration period ("bucket") and can be uniquely associated with a given sequence of the control signals.

In the absence of a signal caused by a particle, the channel should be at a constant pedestal value with fluctuations around this value mostly due to the noise of the chip preamplifier. (The noise introduced in other parts of the chip like the pipeline or the ADC is small. Sensor leakage current shot noise is not relevant before irradiation.) The red points of the figure, at pedestal values close to 100 ADC counts, are indeed fairly constant but at the beginning of digitize and during readout systematic pedestal shifts are observed which exceed the noise level. This data was taken without using the on-chip pedestal subtraction (RTPS), and the maximum pedestal shifts are about 1/2 the size of a Minimum Ionizing Particle's (MIP's) signal.

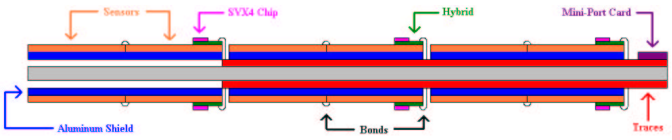

Fig. 3. Simplified side view of a stave. Not to scale.

If the stave is implemented in a particle physics experiment, substantial pedestal fluctuations are bad because the chip cannot distinguish them from a signal caused by a particle crossing the sensor. Thus positive pedestal fluctuations that exceed the set sparsification threshold will cause the particular channel to be read out, causing dead time, fake hits and thus reduced tracking performance. Negative pedestal fluctuations may first seem to be less important. They could however coincide with a real hit, push the particle's signal below the sparsification threshold and thus lead to inefficiency.

In the standard configuration of the SVX4 chip, real-time pedestal subtraction is on. In this mode a special circuitry is effectively subtracting a common offset from all channels during digitization [8]. The value of the offset is determined using the data content of all 128 channels in the given event. The RTPS circuitry exploits that occupancy is typically low and that pickup noise is uniform by most of the 128 channels. Pickup that is effecting only a small number of strips/channels cannot be removed.

Data in RTPS mode taken with the same stave as above are shown as the purple points. First of all the "pedestal" is now substantially lowered. The fact that it is above zero is a nice feature built into the SVX4 RTPS circuitry which allows measurement of an untruncated noise spectrum of a given channel. More importantly, however, the pedestal fluctuations are completely removed.

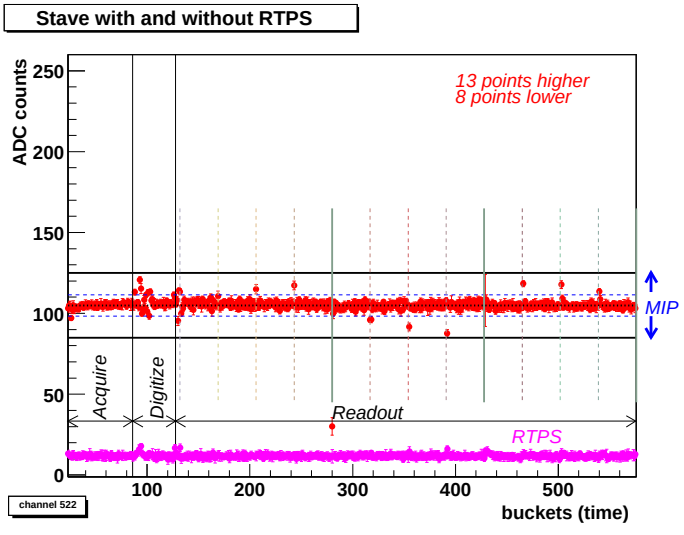

Fig. 4. Illustration of deadtime-less stave performance with (purple) and without (red) real-time pedestal subtraction.

While the current stave deadtime-less performance is likely to be sufficient for operation in a real experiment, it is desirable to understand and suppress any pedestal fluctuation as effectively as possible without relying on the chip's real-time pedestal suppression feature. The mechanisms which may cause systematic pedestal shifts are thus investigated below.

IV. Interference Mechanisms

The stave is a complex electrical system. Some of its main features are sketched in the simplified schematic of Figure 5. The figure shows various parasitic capacitances between power traces, the aluminum shield, and the sensor. It also shows the ground and other connections between sensor ground, analog and digital ground etc. Bond connections are indicated by inductance symbols.

The schematic does not show the other hybrids, the MPC, control or clock lines.

There are four independent interference mechanisms which can couple bus cable activity into the preamplifier and lead to the observed pedestal shifts:

A. Capacitive coupling

Pickup of control signals or voltage fluctuations on the power lines may couple into the high voltage backplane of the silicon sensor. This corresponds effectively to the creation of charge, leads to a pickup signal in the preamplifier, and causes a systematic pedestal shift. The sensor capacitance is in the order of pico Farads and voltage fluctuations as small as a few mV at the high voltage backplane will cause a pickup signal larger than that of an MIP (4 fC).

The best way to reduce these effects is by shielding the bus cable from the sensor by putting the aluminum shield at a fixed potential. The shield's thickness is 25 μm, which was estimated to be sufficient given that the skin depth of aluminum is 25 μm at 10 MHz and 8 μm at 100 MHz.

The effectiveness of the shield is shown in Figure 6. The red points correspond to the situation with a floating aluminum shield (left axis scale). The purple points correspond to a grounded shield (right axis scale). Significant pedestal fluctuations, in particular during digitize, are observed for a floating shield. The position of some of these fluctuations coincides with the arrival of CMOS single-ended control signals needed during digitization, and the position of all peaks is completely understood in terms of data acquisition activity.

If the shield is grounded the pedestal fluctuations during digitize are essentially gone, and a satisfactory performance is achieved.

There are various possible ways to ground the shield. We found it best to connect each of the three shields to the local ground of its corresponding hybrids. Each shield is only connected at one point such that no current flows through the shield. Alternative scenarios, like a common shield for all sensors connected at the MPC ground, have been tested but lead to slightly inferior performance.

Efficient shielding and grounding is the main tool to eliminate capacitive pickup, and significant progress has been achieved. An important technical difficulty that should be mentioned is the creation of a low impedance electrical contact to the shield which is not plated for wire bonding. For the

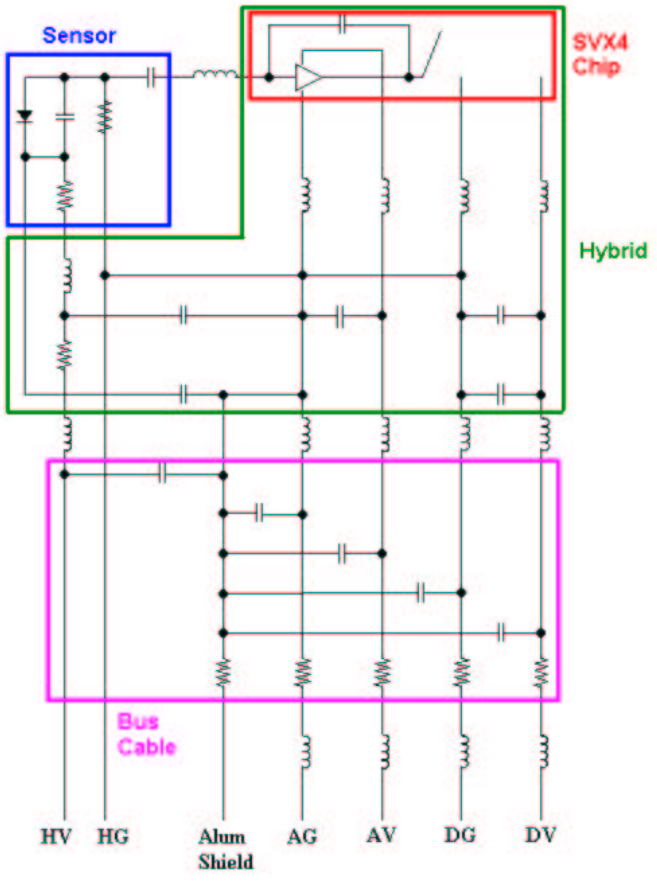

Fig. 5. Sketch of stave simplified schematic

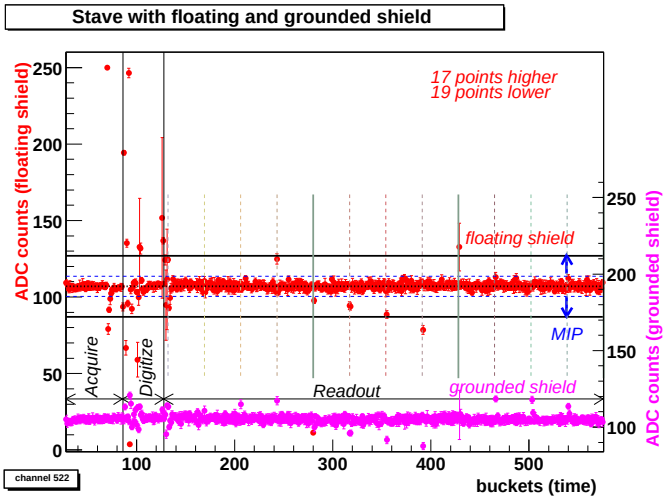

Fig. 6. Stave pedestals recorded with a floating and a grounded shield. In order to distinguish the two cases the vertical axes of the graphs are shifted.

preproduction staves, the shield bond pads on the bus cable have been substantially enlarged, as have the corresponding hybrid ground pads.

There are a number of means other than shielding which have been investigated to suppress capacitive coupling.

For a given signal the coupling strength depends on the impedance $Z = 1/i\omega C$ between bus cable traces and the sensor backplane. Signals with high frequency (ω) components and thus sharp rise and fall times will be most pronounced. The capacitance between trace and sensor back plane depends on geometry, trace width and distance to the sensor, and on the dielectric constant. Some attempts to optimize these stave parameters are still in progress, but the options are limited.

The trace width should be minimized. Currently the trace width is 75 μm for control and clock signals. Reducing it further would cause manufacturing and yield issues, in particular because the cable is long. Increasing the trace distance from the sensor is desirable but also adds material and reduces the heat conduction from the SVX4 chips through (hybrids, sensors,) the bus cable to the stave's cooling pipes. The sensor temperature in the inner layers should be close to -5°C, and the SVX4 chips contribute $\sim$ 50 % of the stave's heat budget.

Reducing the dielectric constant by introducing an air gap is under consideration but again this affects cooling.

Also the logic type and voltage swing on the control signals matter. It would have been preferable to use only differential LVDS control signals for the SVX4 chip. In that case, the net effect of the two signals of opposite polarity would have been much reduced. The presence of a limited number of single-ended control signals on the SVX4 chip was a compromise between position, size, and number of bond pads on a crowded layout.

Lastly, there is some flexibility in the sequence of the SVX4 control signals. This can be exploited to introduce cancellation effects. Some control signals can be raised and dropped within one preamplifier integration cycle or extended over several cycles. Rising and falling control signals cause parasitic charge injections of opposite polarity. Including both edges in one integration cycle can lead to a significant cancellation effect.

B. Conductive coupling

Conductive interference effects arise through the limited impedance of the power lines which cause IR voltage drops if the chip current consumption changes. Since analog, digital and high voltage ground are all tied together on each hybrid, variation of digital or analog current will effectively cause charge injection into the preamplifier input by moving the sensor ground potential.

Unlike the capacitive effects, which are caused by the control signals themselves, the conductive coupling is caused by the effect of these signals on the chip. Shielding cannot mitigate this.

Significant current variations occur when the chip is acquiring data while digitizing and reading out. First, the power consumption is changing at mode transitions like idle/digitize and digitize/readout. Within readout, current consumption changes when data drivers switch on and off, that is at readout priority transitions between different chips and hybrids.

Minimizing the power traces' impedance and thus the size of voltage drops for a given current change is of paramount importance. Again there are tight constraints. The bus cable copper layer contributes significantly to the stave material budget (1.95% of a radiation length) which makes increasing the trace thickness unattractive. (Changes in trace thickness would also affect the impedance of the signal and data lines and require other modifications.)

We thus combined the separate digital ground traces (DG 1-3) of the three hybrids on each side of the stave into one large trace. Also the power traces are widened as much as possible. The digital power traces (DVDD 1-3) remain separate. This is a compromise which allows switching off digital power for individual hybrids in case of failures during operation in the CDF experiment. The analog ground traces of the hybrids are kept separate. This arrangement is sketched in Figure 7. Also shown are the three aluminum shield sections and the connection of the local hybrid ground to the shield under its sensors. The figure shows very clearly that there are a number of ground loops in the system. They are a consequence of the SVX4 chip design and cannot be avoided.

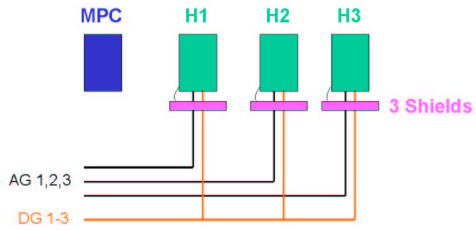

Fig. 7. Sketch of stave analog and digital ground connections and of the shield grounding scheme.

The positive effect of a reduced power trace impedance is shown in Figure 8. The figure shows the pedestal taken for two bonding configurations on the same stave. In the original configuration, the analog and digital power traces of the three hybrids are all separated at the price of having larger impedance (red points, left axis scale). As always, a good performance without pedestal shifts is observed in the first part of the plot, where data is acquired while the chip is not digitizing or reading out. However, during digitize and readout, the pedestal is seen to fluctuate up and down from bucket to bucket, and slowly shift downwards or upwards. The performance in this scenario is clearly unsatisfactory. (The data in this plot has been taken with a floating shield, so the structures discussed above are still present here.)

It should be noted that the slow pedestal shifts during digitize and readout are as bad as faster ones because the sparsification threshold is constant with time. Once set to its preferred value at initialization time, the only thing which determines if a given channel is read out is its ADC count value, not its history.

The purple points in the figure (right axis scale) correspond

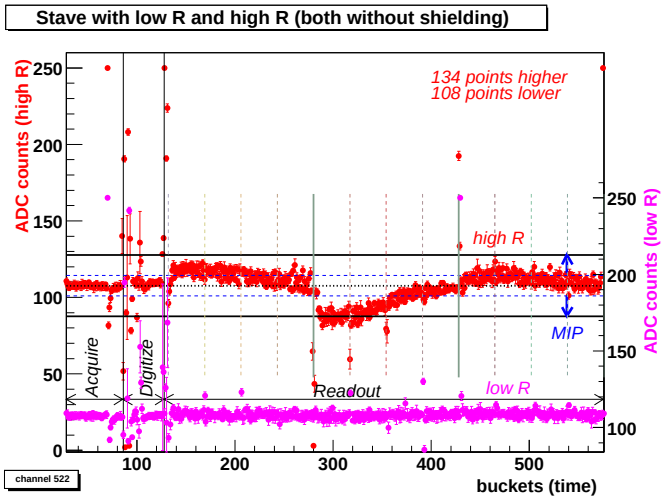

Fig. 8. Stave pedestal for different power trace impedance. In order to distinguish the two cases the vertical axes of the graphs are shifted.

to the same stave modified such that the corresponding power traces of the three hybrids are bonded together (DG 1-3, AG 1-3, DV 1-3, and AV 1-3 are all connected). This reduces trace impedance by approximately a factor of three and gives a much improved performance.

There are a number of additional ways to minimize the effects of conductive interference.

An even more balanced current consumption of the chip would be the most involved way and is excluded in practice.

Strong decoupling of analog and digital power is important and is implemented on the hybrid to the extent the tight space constraints allow. While the hybrid area should be small in order to minimize multiple scattering, the height of components is also limited by mechanical constraints on the barrel bulk heads which carry the staves.

The value of the output data driver currents is a programmable feature of the SVX4 chip. Running with the lowest current leads to a reduced voltage drop and to a significantly reduced pedestal shift during readout. The data signal quality is high such that even the lowest driver current can be used without problems.

C. Inductive interference and electromagnetic radiation

There are two more types of interference mechanisms that could cause pedestal shifts in the system: inductive coupling and (far field) electromagnetic radiation.

These mechanisms do not play a major part in the stave system, and the observed pedestal shifts could all be associated with capacitive and conductive effects.

Far field electromagnetic radiation is not expected to be a major effect. The highest frequencies in the system are less than 1 GHz, and the corresponding wavelengths are typically significantly longer than typical stave dimensions.

At least one stave feature exists, which will in principle cause inductive effects. The geometrical arrangement of the bus cable

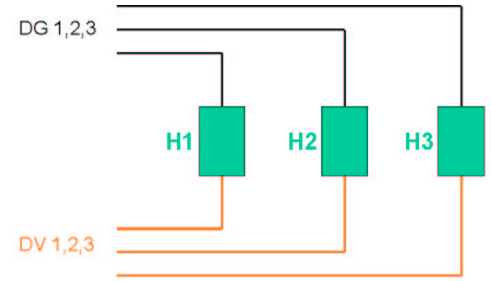

Fig. 9. Arrangement of hybrid digital power traces on the bus cable.

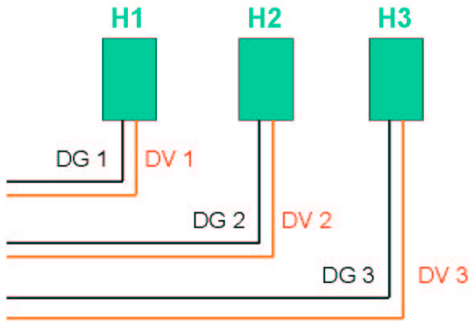

Fig. 10. Alternative arrangement of the digital power traces.

traces providing power to the three hybrids is sketched in Figure 9. The incoming and outgoing power traces of any hybrid form a loop which overlaps with that of the other hybrids. So any current (magnetic flux) change in one of these loops will induce a voltage change in the other ones.

The preferred arrangement is shown in Figure 10 where the loops don't overlap at all. This preferred scenario could not be implemented in the bus cable design without changes in the MPC layout. Instead the loop area was reduced as much as possible.

V. Conclusion

Deadtime-less operation of silicon detectors at hadron colliders provides significant advantages in terms of trigger rates while posing additional challenges for electrical performance. The challenge is further enhanced for very compact and lightweight detector design as is the case for the staves of the CDF Run IIb Silicon Project. CDF built a number of prototype staves, studied their performance in detail, and optimized their design. The stave is a complex electrical system with many constraints imposed by its use in a high luminosity hadron collider experiment.

The main stave features are meanwhile well understood. Stave electrical performance is good and should be sufficient for operation in an experiment, justifying the ambitious design goals.

Further improvements are expected from the preproduction staves that are currently being produced, and early results are very encouraging. These staves use the final version of the SVX4 chip, a modified bus cable design, and different

transceiver chips to drive the control signals, to mention only the major changes that should affect deadtime-less operation.

REFERENCES

[1] M. Aoki *et al.*, CDF Collaboration, "CDF Run IIb Silicon Detector", submitted for Proceedings of the 9th Pisa Meeting on Advanced Detectors, La Biodola, Isola d'Elba (May 25, 2003).

[2] CDF Collaboration, "The CDF IIb Detector: Technical Design Report", FERMILAB-TM-2198 (Feb 2003).

[3] R.-S. Lu *et al.*, CDF Collaboration, "CDF Run IIb Silicon: Stave Design and Testing", submitted for the Proceedings of the IEEE Nuclear Science Symposium 2003, Portland, Oregon.

[4] B. Krieger *et al.*, "SVX4: A New Deep Submicron Readout IC for the Tevatron Collider at Fermilab", ibidem.

[5] G. Cardoso, J. Hoff, A. Shenai and S. Zimmermann, "Ten Bits Differential Transceiver (0.25 μm)", FNAL Note, Document #ESE-SVX-020502 (July 26, 2002).

[6] G. Cardoso *et al.*, "Polyimide and BeO Mini Portcard Performance", submitted for the Proceedings of the IEEE Nuclear Science Symposium 2003, Portland, Oregon.

[7] K. Hara, CDF Collaboration, " Sensors for the CDF Run IIb Silicon Detector", ibidem.

[8] M. Garcia-Sciveres *et al.*, Nucl. Instr. and Meth A435 (1999) 58.